REMARKS

Claims 1 – 12 are pending in the application. Applicants amend claims 1 and 8. No new matter is added. Support may be found, for example, at page 13, lines 22 – 33 of Applicants' specification.

REJECTION UNDER 35. U.S.C. §§ 102, 103

Claims 1 and 2 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,608,662 to Large et al. Claims 8 - 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Large in view of U.S. Patent No. 5,732,233 to Klim et al. Claims 3 - 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Large in view of U.S. Patent No. 6,519,225 to Angle et al. Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Large in view of U.S. Patent No. 6,081,538 to Donley. Applicants amend claims 1 and 8 to clarify the nature of their invention, and respectfully traverse these rejections.

In independent claim 1, Applicants disclose a packet data processing apparatus for processing a packet received from a network by a processor. The apparatus includes a packet data access part, which has a plurality of registers arranged in series, shifting the received packet through the plurality of registers toward an outlet in synchronization with a clock.

The apparatus functions so that the processor processes the received packet while the received packet is being shifted through the plurality of registers, independently of an instruction order for processing the received packet. The processor and the packet data access part are directly connected, and the processor reads out or writes data from or to the packet data access part by synchronizing the cycle time of the processor.

In independent claim 8, Applicants disclose a packet relay a plurality of processors being connected in series so that the packet sequentially passes through the plurality of processors. Each processor includes the packet data access part claimed in claim 1.

In our Response of January 15, 2004, we made the following arguments:

> Large discloses a packet filter engine that shifts received packets through a pipeline register for storage in memory (see, e.g., column 5, line 29 though column 6, line 48 and FIG. 1 of Large). A state machine may selectively process packet bytes extracted from the pipeline register based on an offset from the beginning of the packet (see, e.g., column 5, lines 41 – 54 of Large). However, unlike Applicants' claimed apparatus of claim 1, the device of Large fails to provide a means for the state machine to process portions of the packet while the received packet is being shifted through the plurality of registers. Rather, Large's device allows each byte to be extracted only at its offset position and not as it is being shifted through a plurality of registers.
>
> Klim discloses a high speed pipeline apparatus including a plurality of pipelined processors P_n that each receive data, process data, and then send data on to a next pipeline processor or controller C_n (see, e.g., column 4, lines 1 – 65 of Klim). Unlike Applicants' claimed apparatus of claim 8, the apparatus of Klim does not operate pipelined processors P_n independently of an instruction order for processing the received packet. For example, with reference to FIG. 4 of Klim, Eval_tree a which processes data through pipelined processor P_a is controlled by control signal pc-a from controller C_a, and not by an independent clock synchronization signal.

The Examiner disagrees with this argument, suggesting that adjunct processor 175 of FIG. 1 of Large operates together with memory 170 and system bus 165 to process a received packet while the received packet is being shifted through the plurality of registers.

Notably, Applicants' amended claims 1 and 8 require that the processor and the packet data access part are directly connected, and that the processor reads data out from and writes data to the packet data access part by synchronizing the cycle time of the processor. As a result, overhead associated with conventional reading/writing operations to memory is eliminated, and reading and writing can proceed at very high speeds (see, e.g., page 13, lines 29 – 33 of Applicants' specification).

Adjunct processor 175 of Large writes to memory 170 via system bus 165 while a received packet is being shifted through registers 130 (see, e.g., FIG. 1 of Large). In sharp contrast to Applicants' claimed invention, this configuration represents a conventional approach (for example, as described in Applicants' specification at page 4, lines 27 – 31) that fails to achieve the high speed performance of Applicants' claimed approach through direct connection and synchronization of shifting in registers 130 with the cycle time of the processor.

Moreover, processor 175 of Large fails to meet the limitations of Applicants' claimed invention by processing a different data packet than is simultaneously processed through registers 130 (see, e.g., column 10, lines 16 – 19 and column 12, lines 61 - 64 of Large, respectively describing notification and transfer of an accepted packet shifted through registers 130 to processor 175). In sharp contrast, Applicants a processor that processes a received packet "while the received packet is being shifted through the plurality of registers".

By means of processor 175, the Examiner suggests that the configuration of Large is able to "process portions of the packet while the received packet is being shifter through the plurality of registers". However, the packet processed by processor 175 at a given time is clearly different from the received packet being processed through registers 130.

In addition unlike Applicants' claimed invention, neither state machine 100 nor adjunct processor 175 have any means for means for directly writing information to pipeline registers 130. For example, FIG. 1 and the specification of Large fail to disclose or suggest a signal line from state machine 100 to registers 130 that would facilitate state machine 100 directly writing to registers 130. While state machine 100 is able to keep track of a position of a packet in registers 130 by means of an offset counter (see, e.g., column 5, lines 40 – 54 of Large), it is not possible for state machine 100 to directly access data at intermediate positions in registers 130,

as is required for rewriting packet data via Applicants' packet data access part (for example, in order to write a checksum re-calculation result to an IP header after shifting to the end of the header). Moreover, Large fails to disclose or suggest a direct means by which processor 175 is able to write to registers 130.

In addition, Applicants submit that the combination of Klim and Large also fails to disclose or otherwise suggest the above-described limitations of Applicants' independent claims 1 and 8.

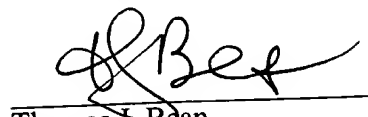
Accordingly, Applicants respectfully submit that independent claims 1 and 8 are not anticipated or made obvious by either of Large and Klim, and are therefore in condition for allowance. As claims 2 – 7 and 9 – 12 each depend from one of allowable claims 1 and 8, Applicant respectfully submits that claims 2 – 7 and 9 – 12 are also allowable for at least this reason.

CONCLUSION

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that claims 1 – 12, consisting of independent claims 1 and 8, and the claims dependent therefrom, are in condition for allowance. Passage of this case to allowance is earnestly solicited. However, if for any reason the Examiner should consider this application not to be in condition for allowance, she is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,



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